

Labs : Real-Time Scheduling Tools

ETR 2015

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Summary

- Few words about real-time scheduling tools**
- Introducing Cheddar**
- Labs**

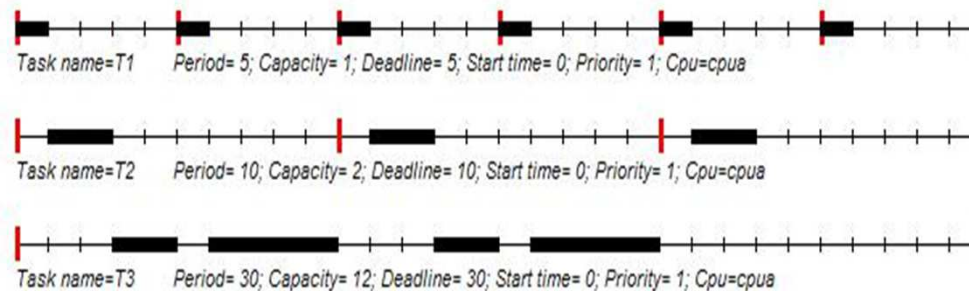
Real-Time Scheduling Analysis Tools

- MAST** (<http://mast.unican.es/>).
- Rapid-RMA** (<http://www.tripac.com/>).
- SymTA/S** (<https://www.symtavision.com>)
- STORM** (<http://storm.rts-software.org/doku.php>)
- SchedMCore** (<http://sites.onera.fr/schedmcore/>)
- Simso** (<http://projects.laas.fr/simso/>)
- YARTISS** (<http://igm.univ-mlv.fr/rtalgo/Softwares/YARTISS>)
- SYNDEX** (<http://www.syndex.org>)
- RTSIM** (<http://rtsim.ssup.it>)
- RT-Druid** (<http://www.evidence.eu.com/products/rt-druid.html>)
- AADLInspector** (<http://www.ellidiss.fr/public/wiki/wiki/inspector>)
- Cheddar** (<http://beru.univ-brest.fr/svn/CHEDDAR>)
- ...

Real-Time Scheduling Analysis Tools

1. Modeling the architecture, ADL

2. Scheduling Simulation



3. Feasibility tests. E.g. Joseph and Pandia WCRT

$$R_i = C_i + \sum_{j \in hp(i)} \left\lceil \frac{R_i}{P_j} \right\rceil \cdot C_j$$

4. Optimization, architecture exploration

There are some tools ... but

1. Require deep real-time scheduling analysis theory skills :

- Numerous theoretical results and assumptions. How to choose ?
- Sometimes require to abstract the system to verify. How ?
- Pessimism, scheduling anomalies

2. Relationships with engineering process:

- Relationships with design languages (design pattern) and programming language/operating systems features (Ada Ravenscar)
- When and how to use them ? WCET ?

3. Less methods/tools for some architectures: multi-core, distributed, hierarchical systems, many-core, functions ...

4. ...

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Introducing Cheddar

- ❑ **Open source teaching tool, with few commercial examples of use :**
AADLInspector (Ellidiss Tech.), TASTE (ESA), ...
 1. <http://www.ellidiss.fr/public/wiki/wiki/inspector>
 2. <http://beru.univ-brest.fr/~singhoff/cheddar>

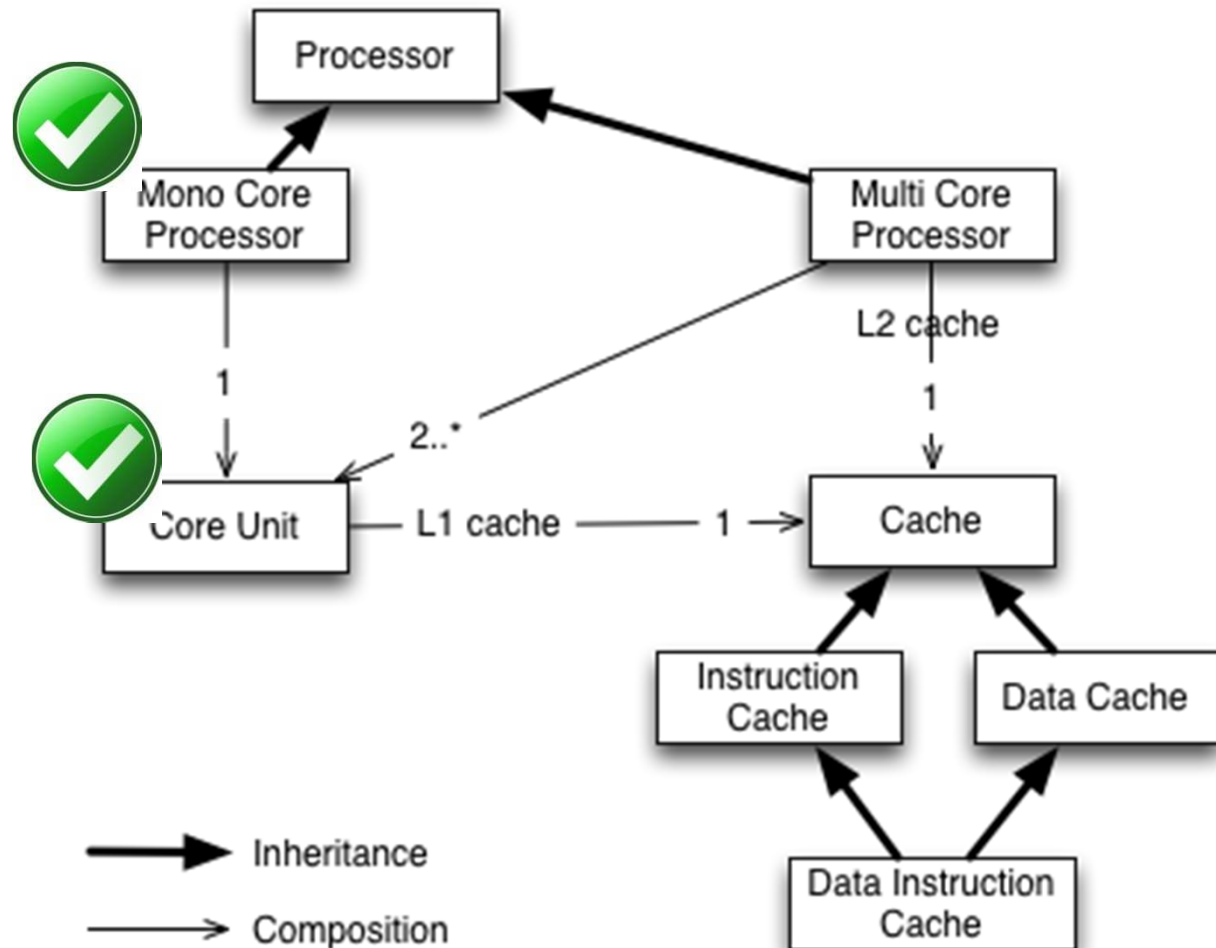
- ❑ **Architecture modeling :** Cheddar ADL, but designs are expected to be expressed with standard architecture design languages : AADL, UML MARTE.
 - ❑ ADL to implement analysis algorithms, semantic & legality rules, textual representation (XML), model-driven
 - ❑ Light Cheddar ADL editor, for teaching purpose only

- ❑ **Sponsors/Contributors :** Ellidiss Tech, Lab-STICC, Campus France, UBO, BMO, Région Bretagne, CG Finistère, BPI France, Thalès TCS, Télécom Paris Tech, ISAE, Univ. Lisboa, IUC

Cheddar ADL

Component types:

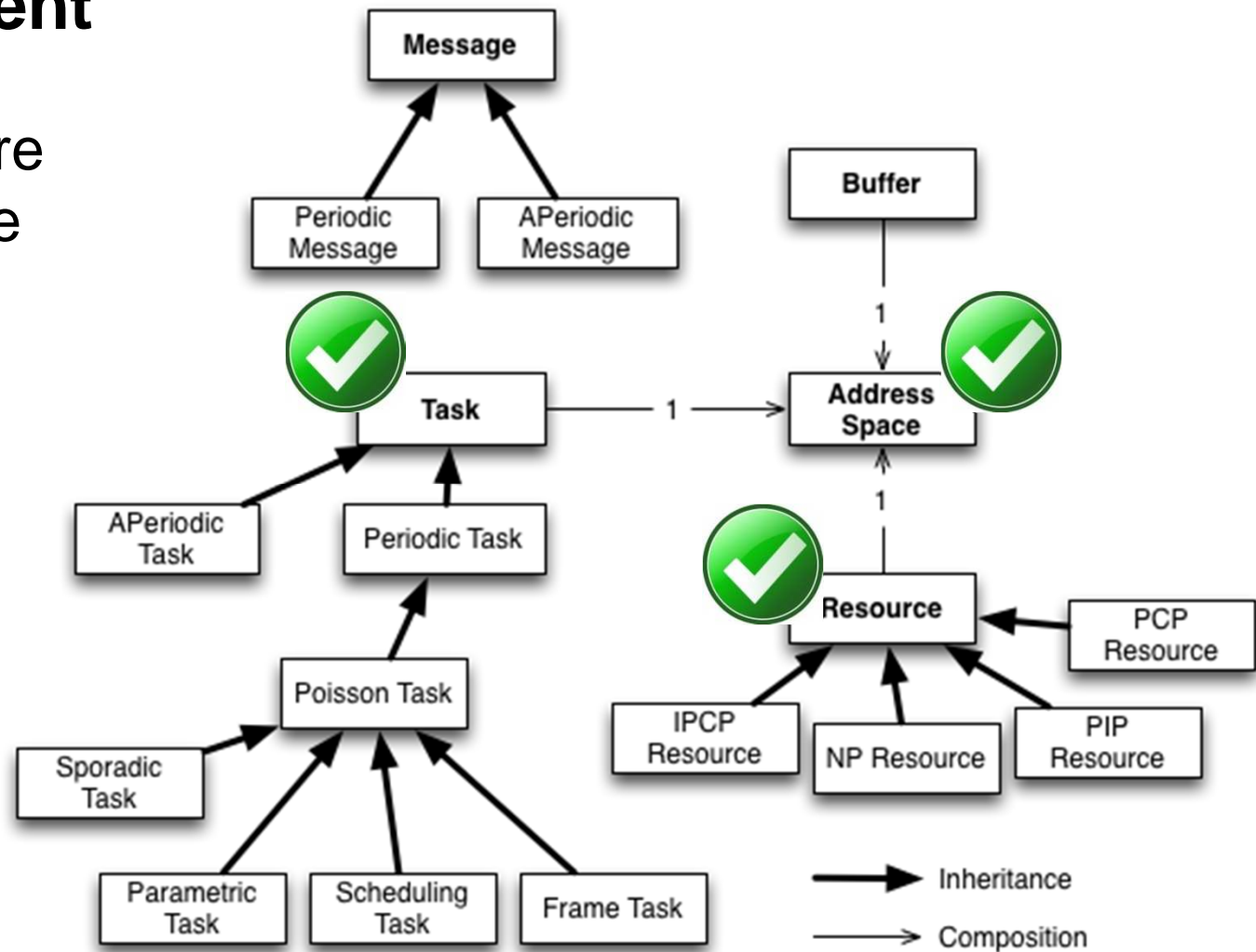
- Hardware
- Software



Cheddar ADL

❑ Component types:

- ❑ Hardware
- ❑ Software



Analysis



1. Simulation :

- Various uniprocessor/multicore/hierarchical schedulers, task model (periodic, sporadic, aperiodic, poisson process, multi frame), cache, resources, buffer, message, user defined policies
- Worst/best/average task response time, resource blocking time, number of preemption, context switches, deadlock, priority inversion, buffer usage ...

2. Feasibility tests :

- Periodic & transaction & holistic WCRT, queuing analysis, resource blocking times, CRPD/UCB, ...

3. Architecture exploration, optimization:

- Verify an architecture model, improve model, verify, improve, ...
- Task priority/deadline assignment, partitioning, design-pattern analysis, task clustering
- PAES optimization

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Toolset environment

Where to find the exercises :

<http://etr2015.irisa.fr/index.php/travaux-pratiques>

How to set the workspace for this lab :

- Define and start a Linux/ubuntu VirtualBox VM with *cheddar_tutorial_french_ubuntu.vdi*
- Login : cheddar ; Password : cheddar*
- source cheddar.bash*
- cheddar &*

Solutions ? Full software ?

- Next week, on the same web page

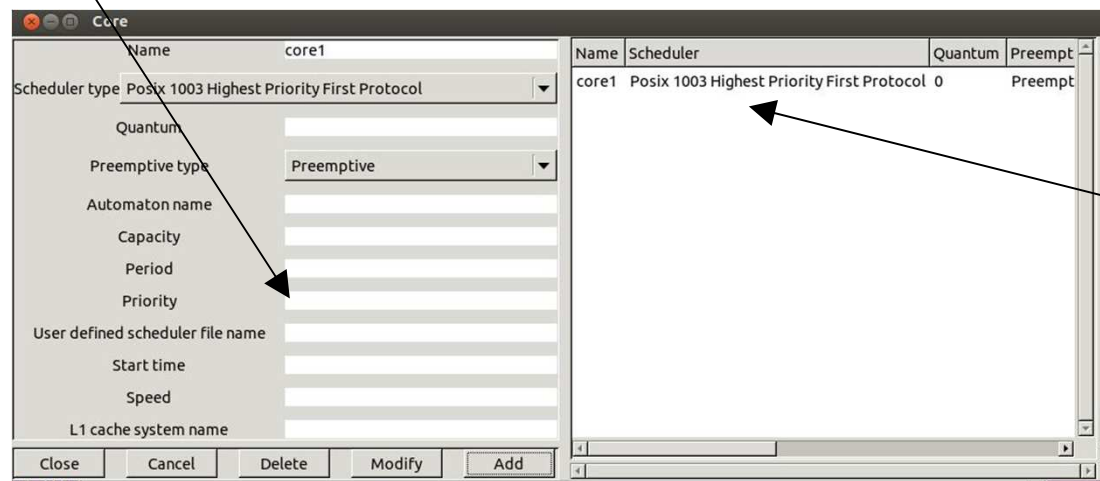
Exercise summary

- ❑ **Exercise 1** : an example of use
- ❑ **Exercises 2, 3** : EDF vs fixed priority vs LLF
- ❑ **Exercises 4 and 5** : shared resources, inversion priority, PIP and PCP
- ❑ **Exercises 6 and 7** : two case studies

Design and verification of a model

Attributes

Entity name

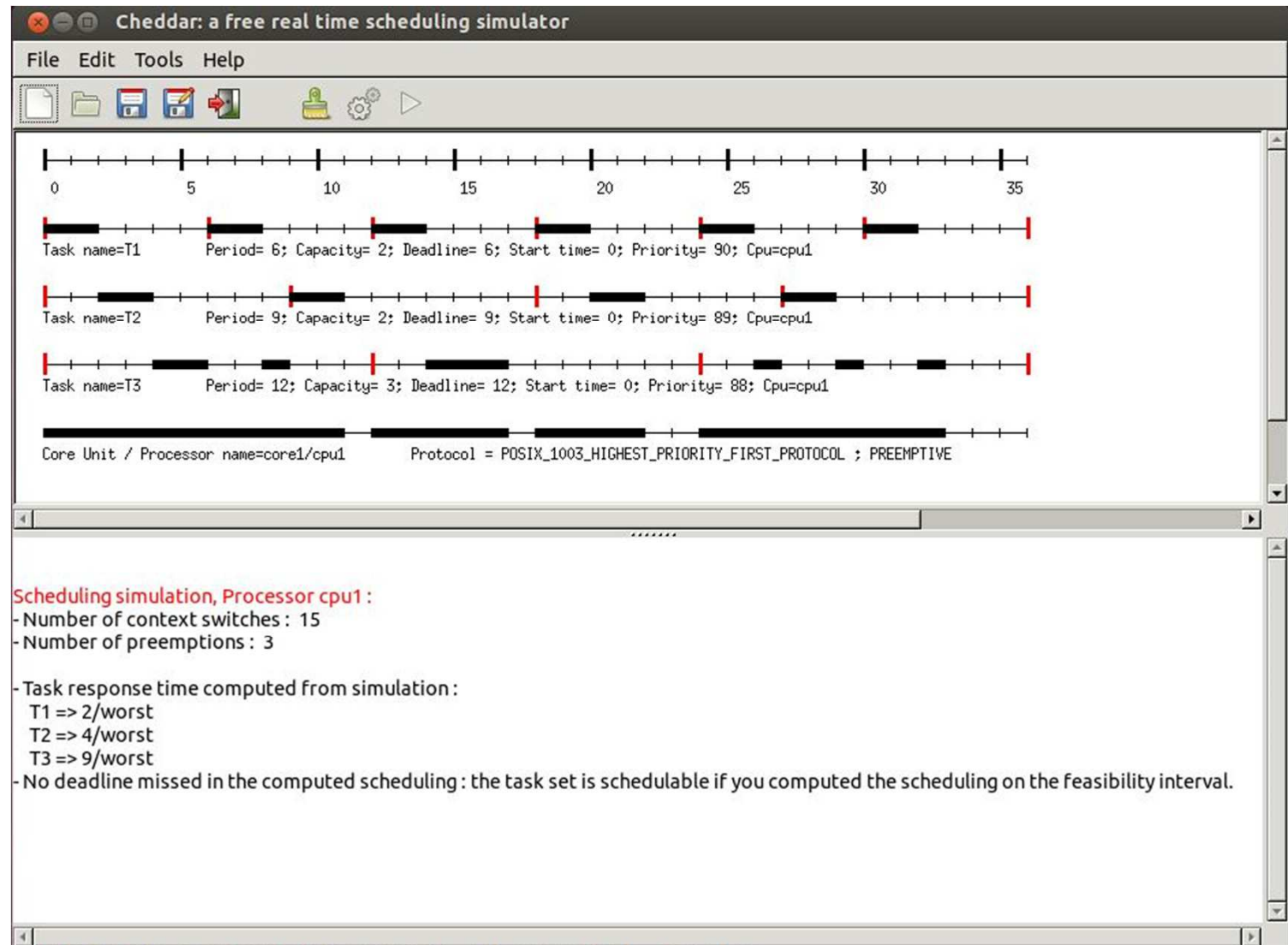


Existing entities, click the line before editing

- ❑ **Update set of entities and their attribute values**
- ❑ **Buttons** : Close, Cancel, Delete, Modify, Add
- ❑ **Example** : core component “*core1*”, POSIX scheduling

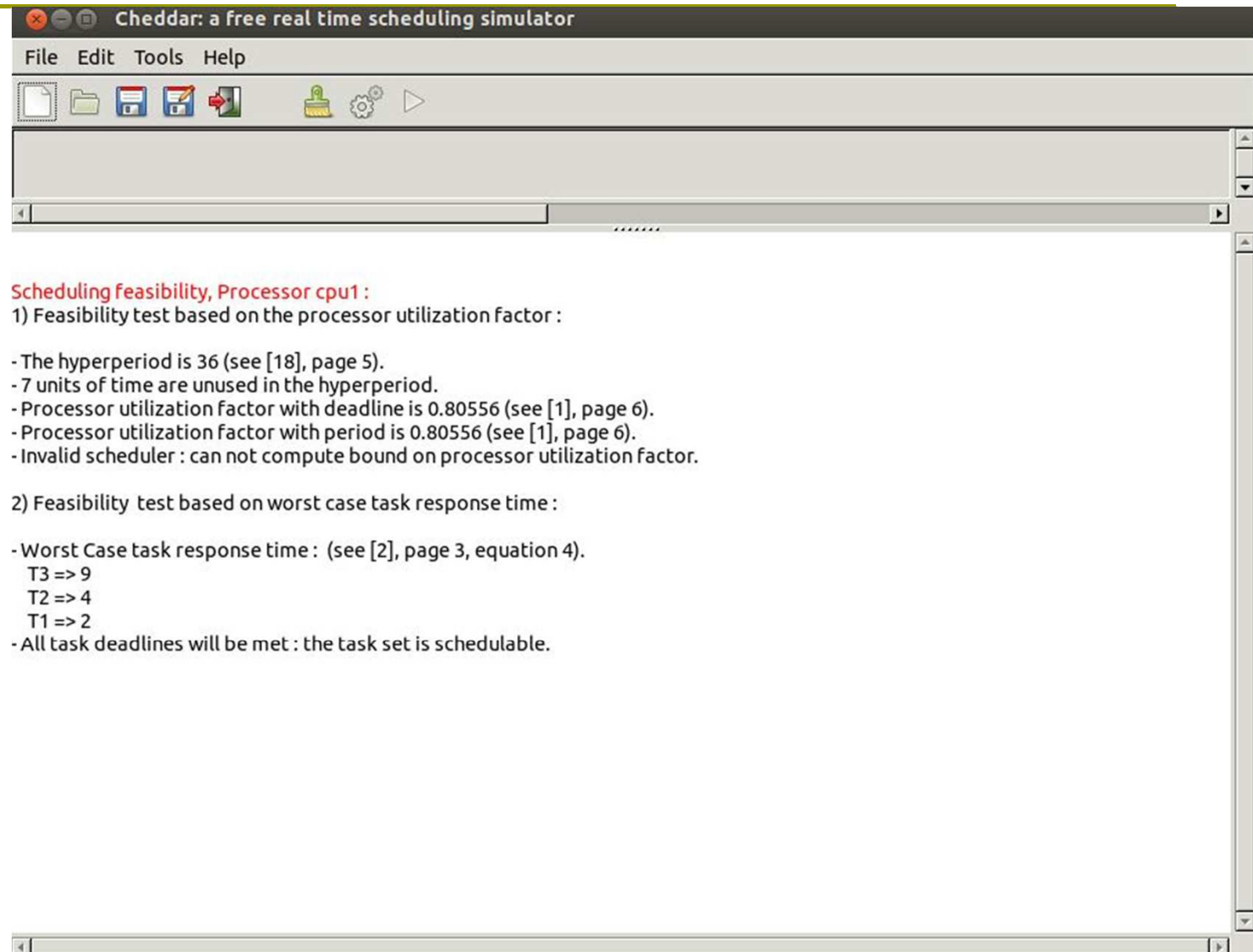
Design and verification of a model

Simulation results



Design and verification of a model

Feasibility test results



Cheddar: a free real time scheduling simulator

File Edit Tools Help

Scheduling Feasibility, Processor cpu1 :

1) Feasibility test based on the processor utilization factor :

- The hyperperiod is 36 (see [18], page 5).
- 7 units of time are unused in the hyperperiod.
- Processor utilization factor with deadline is 0.80556 (see [1], page 6).
- Processor utilization factor with period is 0.80556 (see [1], page 6).
- Invalid scheduler : can not compute bound on processor utilization factor.

2) Feasibility test based on worst case task response time :

- Worst Case task response time : (see [2], page 3, equation 4).
 - T3 => 9
 - T2 => 4
 - T1 => 2
- All task deadlines will be met : the task set is schedulable.